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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Steinhoff et al.**
Serial No.: **09/498,677**
Filed: **02/07/2000**

Docket Number: **TI-29599**
Art Unit: **3663**
Examiner: **Johannes P. Mondt**
Conf. No.: **9140**

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November 17, 2008
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___ CONTINUATION APP'N (# Pages)	
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NAME OF INVENTOR(S): *Steinhoff et al.*	RECEIPT DATE & SERIAL NO.: *09/ 498,677*
	FILING DATE: *February 7, 2000*
TITLE OF INVENTION: *BI-DIRECTIONAL ESD PROTECTION CIRCUIT*	
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For: **BI-DIRECTIONAL ESD PROTECTION CIRCUIT**

APPELLANTS' BRIEF

November 17, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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I hereby certify that the above correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office on November 17, 2008.

Robert N. Rountree

Robert N. Rountree, Reg. No. 39,347

Dear Sir:

In support of their appeal of the Final Rejection of claims in the above-referenced application, Appellants respectfully submit herein their brief. In response to the Notification of Non-Compliant Appeal Brief mailed October 22, 2008, please replace the Appeal Brief filed May 12, 2008, with the instant Appeal Brief.

1. REAL PARTY IN INTEREST

Texas Instruments Incorporated is the real party in interest.

2. RELATED APPEALS AND INTERFERENCES

No other related appeals or interferences are known to Appellants.

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3. STATUS OF CLAIMS

Claims 1-13 are in the application. Claims 1-2, 6-7, and 11-12 are rejected under 35 U.S.C. § 102(e). Claims 3-5, 8-10, and 13 are rejected under 35 U.S.C. § 103(a). Examiner, in an Office Action of June 11, 2007, made final rejection of claims 1-13. Examiner reaffirmed the June 11, 2007 rejection in an Advisory Action dated November 23, 2007. Claims 1-13 are on appeal and are reproduced in the Appendix to Appellants' Brief filed herewith.

4. STATUS OF AMENDMENTS

An amendment was filed after final rejection on November 9, 2007. Examiner refused to enter the amendment. The amendment is hereby withdrawn.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to a structure, which is preferably used for electrostatic discharge (ESD) protection. A preferred embodiment of this structure is illustrated at Figures 1A through 1C and described at page 1, line 18 through page 8, line 2. Referring to Figure 1A, the structure includes an external terminal 100 and a reference terminal 102. (page 4, lines 20-21). A first transistor 106 is formed on a substrate 171 (Figure 1C). The first transistor has a current path electrically connected between the external terminal 100 and the reference terminal 102. (page 4, lines 20-21). A second transistor 118 has a current path electrically connected between the external terminal 100 and the substrate 108. A third transistor 120 has a current path electrically connected between the substrate 108 and the reference terminal 102. The current paths of the second and third transistors are in parallel with the current path of the first transistor. Note that the drain of transistor 118 is connected to the drain of transistor 106 via resistor 114, and the source of transistor 120 is connected to the source of transistor 106 via resistor 116. (page 4, lines 22-26).

During normal operation, the primary protection transistor 106 is held off by either transistor 118 or transistor 120. (page 6, lines 7-20). During ESD operation, a positive pulse at

external terminal 100 with respect to reference terminal 102 couples a positive voltage to substrate 171 via the gate-to-drain capacitance of transistor 106. This serves to forward bias the parasitic NPN transistor of MOS transistor 106, to initiate snapback conduction. Snapback conduction (BV_{CEO}) provides a very low impedance current path through transistor 106 to discharge the ESD voltage (charge) at external terminal 100 to reference terminal 102). (page 6, line 22 through page 7, line 6). Application of a negative ESD pulse at external terminal 100 with respect to reference terminal 102 operates as previously described except for the polarity reversal and change of ESD current direction through transistor 106. (page 7, lines 8-22). Advantages of the present invention are described at page 7, line 24 through page 8, line 2.

6. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-2, 6-7, and 11-12 are rejected under 35 U.S.C. § 102(e) as being anticipated by Williamson (U.S. Pat. No. 6,369,427).

B. Claims 3-5, 8-10, and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Williamson (U.S. Pat. No. 6,369,427) in view of Williams (U.S. Pat. No. 6,060,752).

C. Claim 13 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Williamson (U.S. Pat. No. 6,369,427) in view of Maeda (U.S. Pat. No. 5,976,921).

7. ARGUMENT

A. Claim 1 is rejected under 35 U.S.C. § 102(2) as being anticipated by Williamson (U.S. Pat. No. 6,369,427). Claim 1 recites "A structure, comprising: an external terminal; a reference terminal; **a first transistor formed on a substrate**, the first transistor having a current path electrically connected between the external terminal and the reference terminal; **a second transistor having a current path electrically connected between the external terminal and the substrate**; and **a third transistor having a current path electrically connected between**

the substrate and the reference terminal, wherein **the current paths of the second and third transistors are in parallel with the current path of the first transistor.**" (emphasis added).

In a final rejection of June 11, 2007, with reference to Figure 5 of Williamson, Examiner has identified transistor 56 as the first transistor, the p-type transistor in 44 as the second transistor, and the n-type transistor in 44 as the third transistor. With reference to connectivity, Examiner identifies "a second transistor (p-type transistor in 44) having a current path electrically connected between the substrate (through node 66 and electrical connection with resistor 42 connecting to a terminal common to the two transistors in 44: see Figure 5) (col. 6, l. 17-31); a third transistor (n-type transistor in 44) having a current path electrically connected between the substrate (through node 66 and electrical connection with resistor 42 connecting to a terminal (ground) (see Figure 5) (col. 6, l. 17-31)." (Office Action 6/11/2007, page 3). Examiner further states "Furthermore, 'electrically connected' does include the case of capacitive coupling." (Office Action 6/11/2007, page 7). The Honorable Board will appreciate that this rejection is somewhat confusing, because Examiner omits key parts of claim 1 and states that the second and third transistors are connected "between the substrate." Furthermore, the parenthetical expression "(through node 66 and electrical connection with resistor 42 connecting to a terminal common to the two transistors in 44: see Figure 5)" does not explain how the second transistor has "a current path electrically connected between the external terminal and the substrate" or how the third transistor has "a current path electrically connected between the substrate and the reference terminal" as required by claim 1. Appellants believe that Examiner has interpreted substrate connections recited in claim 1 as capacitive coupling between source or drain regions of the p-type and n-type transistors in 44 (Figure 5 of Williamson). In either case, however, Williamson fails to anticipate claim 1 and depending claims 2, 6-7, and 11-12 for the following reasons.

First, neither the p-type transistor nor the n-type transistor in 44 of Williamson has "a current path electrically connected between the external terminal and the substrate" (second transistor) or "a current path electrically connected between the substrate and the reference terminal" (third transistor) as required by claim 1. In the embodiment of Figure 1A of the present invention, the current path of each of the first and second transistors must be between their

respective source and drain regions if they are in parallel with the current path of the first transistor. If capacitive coupling between source/drain regions and the substrate of Williamson is taken as the current path recited in claim 1, then the current paths of the second and third transistors are not in parallel with the current path of the first transistor, which is "electrically connected between the external terminal and the reference terminal."

Second, the second and third transistors of claim 1 have current paths that are electrically connected to the same substrate. The p-type and n-type transistors of Williamson (Figure 5 in 44) have source/drain regions that are capacitively coupled to different substrates. The p-type transistor must be formed on an n-type substrate and the n-type transistor must be formed on a p-type substrate. Otherwise, the source/drain regions of the offending transistor would be shorted.

Third, if "electrically connected" includes the case of capacitive coupling as Examiner contends (Office Action 6/11/2007, page 7), then it is impossible to claim electrical connection of any circuit, since all elements are capacitively coupled to each other. For example, the claims of Williamson simply recite that elements are "coupled." Should Williamson be reexamined? Moreover, transistors would have an unlimited number of current paths through this capacitive coupling. Such an absurd result flows from an overly broad interpretation of claim limitations without regard to the instant specification or the present invention described therein. Thus, claim 1 and depending claims 2, 6-7, and 11-12 are patentable under 35 U.S.C. § 102(e).

Claim 2 depends from claim 1 and recites "a first resistor 114 coupled between the external terminal (100) and the current path of the second transistor 118; and a second resistor 116 coupled between the current path of the third transistor 120 and the reference terminal 102." (Figure 1A, reference numerals added). Examiner states "(either the inherently present contact resistance caused by the contact made between the gate and the source/drain in said second transistor (p-type transistor in 44), or, in an alternative, resistor 42." (Office Action 6/11/2007, page 3). Claim 2 specifically recites first and second resistors. This is not the same as contact resistance. Moreover, the only inherent contact resistance between the gate and source/drain regions of the p-type transistor in 44 (see source-to-gate connection of p-type transistor in 44) is

not part of the current path unless the gate is shorted to the source/drain region. In the alternative, Examiner cites resistor 42 as anticipating both the first and second resistors of claim 2. But only one resistor 42 is disclosed by Williamson. Resistor 42 could not possibly anticipate both the first and second resistors of claim 2. Thus, claim 2 is patentable under 35 U.S.C. § 102(e).

Claim 6 depends from claim 1 and recites "the first transistor further comprises a control terminal electrically connected to the substrate." In the embodiment of Figure 1A, the control terminal of transistor 106 really is electrically connected to the substrate 108. (page 5, lines 26-28). Examiner again resorts to "capacitively" coupled to identify this missing claim limitation. (Office Action 6/11/2007, page 4). This interpretation leads to the conclusion that all n-type transistor control gates are electrically connected to the substrate and, therefore, electrically connected to each other. Moreover, all control gates must also be electrically connected to their own source/drain regions as well as all other source/drain regions. Appellants pray that the Honorable Board will understand that it is impossible to draft circuit claims under this overly broad interpretation. Thus, claim 6 is patentable under 35 U.S.C. § 102(e).

Claim 7 depends from claim 6 and recites substantially the same limitations as claim 2 as previously discussed. Thus, claim 7 is patentable under 35 U.S.C. § 102(e).

Claim 12 depends from claim 1 and recites "the first transistor is an MOS transistor having a control gate electrically connected to the substrate." Examiner again relies on "capacitive coupling" between the control gate and substrate to identify this missing claim limitation. Therefore, Appellants reiterate their previous argument with regard to claim 6. Thus, claim 12 is patentable under 35 U.S.C. § 102(e).

B. Claims 3-5, 8-10, and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Williamson (U.S. Pat. No. 6,369,427) in view of Williams (U.S. Pat. No. 6,060,752). Claims 3-5, 8-10, and 13 are patentable under 35 U.S.C. § 103(a) as depending from patentable claim 1.

Claim 4 depends from claim 3, which depends from claim 1. Referring to the embodiment of Figure 1C, claim 3 recites "the substrate 171 is a first lightly doped region having a first conductivity type." According to claim 1, the first transistor 106 is formed on this first lightly doped region. Claim 4 further recites "a first heavily doped region 170 having a second conductivity type and **underlying the substrate and the first transistor**; and a second lightly doped region 104 having the second conductivity type, the second lightly doped region formed at a face of the substrate and extending to the first heavily doped region." (identification numerals and emphasis added). Contrary to Examiner's assertion, there is no first transistor formed on substrate 900 of Williams. Moreover, neither of NBL layers 926 or 928 is under substrate 900. Thus, claim 4 is patentable under 35 U.S.C. § 103(a).

Claim 8 depends from claim 7 and includes substantially the same limitations as claims 3-4. Thus, for the same reasons, claim 8 is patentable under 35 U.S.C. § 103(a). Claims 9-10 are patentable under 35 U.S.C. § 103(a) as depending from patentable claim 8.

C. Claim 13 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Williamson (U.S. Pat. No. 6,369,427) in view of Maeda (U.S. Pat. No. 5,976,921). If an independent claim is nonobvious under 35 U.S.C. § 103(a), then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Claim 13 depends from claim 1 and is, therefore, patentable as depending from a patentable base claim.

Furthermore, claim 13 recites "[a] structure as in claim 1, wherein the first transistor is a bipolar transistor having a base terminal electrically connected to the substrate." Examiner cites col. 13, lines 48-65 (Figures 1-2), and col. 14, lines 40-52 (Figure 8), of Maeda as disclosing a bipolar transistor having a base terminal connected to the substrate. The Honorable Board will appreciate that Maeda discloses a vertical NPN transistor of a BiCMOS process at Figures 1-2 and 8. The BiCMOS process of Maeda is incompatible with the CMOS process of Williamson. One of ordinary skill in the art at the time of the present invention would not think to combine elements from two incompatible processes to produce the invention of claim 13.

Moreover, there is no teaching or suggestion in either reference to indicate how or why the second and third series-connected transistors of claim 13 might have current paths connected to the base of the first transistor and in parallel with a current path of the first transistor. This is simply a matter of Examiner's impermissible hindsight. Appellants respectfully submit "[t]he references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention." *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986). Thus, claim 13 is patentable under 35 U.S.C. § 103(a) over Williamson (U.S. Pat. No. 6,369,427) in view of Maeda (U.S. Pat. No. 5,976,921).

For all the foregoing reasons, Appellants pray that the Honorable Board will find Examiner has erred and find claims 1-13 patentable over the cited references.

8. CLAIMS APPENDIX

1. (Previously amended) A structure, comprising:

an external terminal;

a reference terminal;

a first transistor formed on a substrate, the first transistor having a current path electrically connected between the external terminal and the reference terminal;

a second transistor having a current path electrically connected between the external terminal and the substrate; and

a third transistor having a current path electrically connected between the substrate and the reference terminal, wherein the current paths of the second and third transistors are in parallel with the current path of the first transistor.

2. (Original) A structure as in claim 1, further comprising:

a first resistor coupled between the external terminal and the current path of the second transistor; and

a second resistor coupled between the current path of the third transistor and the reference terminal.

3. (Original) A structure as in claim 1, wherein the substrate is a first lightly doped region having a first conductivity type.

4. (Original) A structure as in claim 3, further comprising:

a first heavily doped region having a second conductivity type and underlying the substrate and the first transistor; and

a second lightly doped region having the second conductivity type, the second lightly doped region formed at a face of the substrate and extending to the first heavily doped region.

5. (Original) A structure as in claim 4, further comprising:

a first diode coupled between the external terminal and the second lightly doped region; and

a second diode coupled between the reference terminal and the second lightly doped region.

6. (Previously amended) A structure as in claim 1, wherein the first transistor further comprises a control terminal electrically connected to the substrate.

7. (Original) A structure as in claim 6, further comprising:

a first resistor coupled between the external terminal and the current path of the second transistor; and

a second resistor coupled between the current path of the third transistor and the reference terminal.

8. (Original) A structure as in claim 7, wherein the substrate is a first lightly doped region having a first conductivity type, the structure further comprising:

a first heavily doped region having a second conductivity type and underlying the substrate and the first transistor; and

a second lightly doped region having the second conductivity type, the second lightly doped region formed at a face of the substrate and extending to the first heavily doped region.

9. (Original) A structure as in claim 8, further comprising:

a first diode having a first terminal coupled to the second lightly doped region and having a second terminal coupled between the first resistor and the current path of the second transistor; and

a second diode having a first terminal coupled to the second lightly doped region and having a second terminal coupled between the second resistor and the current path of the third transistor.

10. (Original) A structure as in claim 9, further comprising:

an isolation circuit connected to the external terminal; and

a protected circuit electrically connected to the isolation circuit.

11. (Original) A structure as in claim 1, further comprising a protected circuit electrically connected to the external terminal.

12. (Previously amended) A structure as in claim 1, wherein the first transistor is an MOS transistor having a control gate electrically connected to the substrate.

13. (Previously amended) A structure as in claim 1, wherein the first transistor is a bipolar transistor having a base terminal electrically connected to the substrate.

9. EVIDENCE APPENDIX

None.

10. RELATED PROCEEDINGS APPENDIX

None.

Respectfully submitted,

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